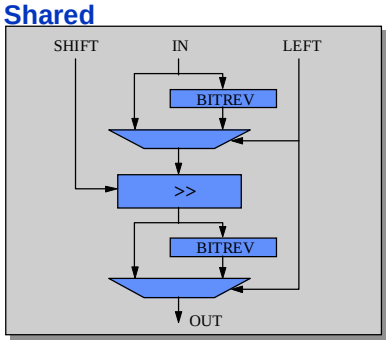
Architectural Trade-Offs

Conceptual View

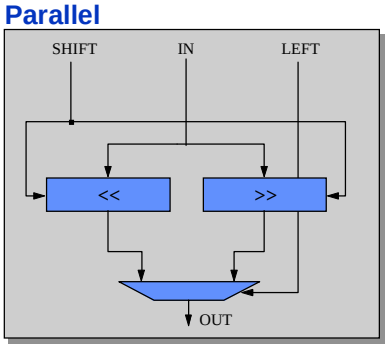
Module Compiler Code

Shared



XIN = LEFT ? bitrev(IN) : IN;
XOUT = XIN >> SHIFT;
OUT = LEFT ? bitrev(XOUT) : XOUT;

Parallel



wire [width] z_left = a<<shift;
wire [width] z_right = a>>shift;
z = left ? z_left : z_right ;

	Area (gates)	Delay (ns)	RT (min)	Comments
Shared	258	2.05	< 1	32-bit data, 5-bit shift
Parallel	398	1.86	< 1	32-bit data, 5-bit shift

Using .25u, 3.3V process, worst-case operating condition

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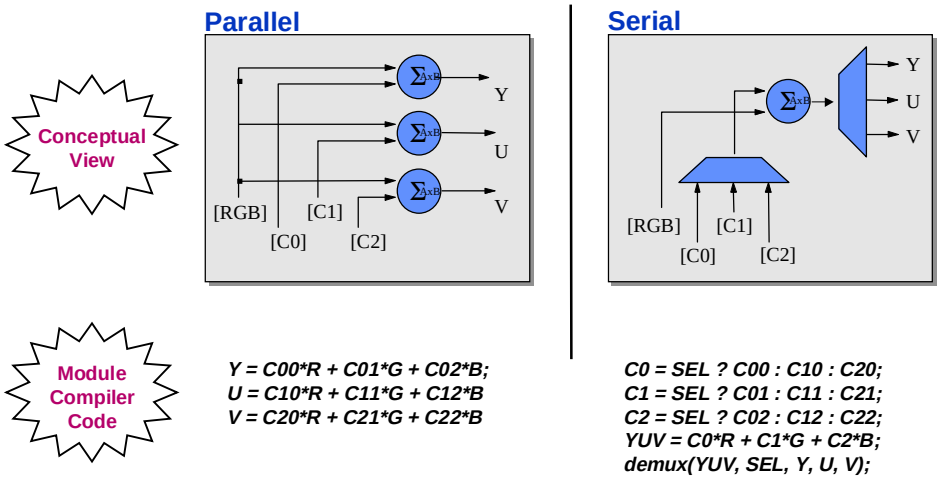

	Area (gates)	Delay (ns)	RT (min)	Comments
Parallel	589	3.19	< 1	8-bit data; constant coeffs
Serial	986	5.05	< 1	8-bit data; constant coeffs
Parallel	2356	4.66	< 1	8-bit data; **variable** coeffs

Using .25u, 3.3V process, worst-case operating condition

1-2

Notice that the parallel architecture is *smaller* than the serial.

This is because the design uses constant coefficients and these multipliers are relatively inexpensive. With the serial architecture, the constant coefficients go through some multiplexing and are no longer constant.

If the coefficients are *variable*, the parallel architecture gets much larger.